Search Results -

Terms	Documents
L1 same multiple same (empt\$3 or free)	5

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result set

DB=PGPB; PLUR=YES; OP=OR

<u>L2</u> L1 same multiple same (empt\$3 or free)

5 L2

<u>L1</u> synchronous\$3 same asynchronous\$3 same (rate or speed)

1790 L1

Search Results -

Terms	Documents	
L4 and bridge	0	

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DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L6</u> L4 and bridge	0	<u>L6</u>
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L5</u> L4 and bridge	31	<u>L5</u>
<u>L4</u> L1 same multiple	231	<u>L4</u>
<u>L3</u> L1 same multiple same (empt\$3 or free)	5	<u>L3</u>
DB=PGPB; PLUR=YES; OP=OR		
<u>L2</u> L1 same multiple same (empt\$3 or free)	· 5	<u>L2</u>
<u>L1</u> synchronous\$3 same asynchronous\$3 same (rate or speed)	1790	<u>L1</u>

Search Results -

Terms	Documents
(375/354 370/230 370/232 370/235 370/401 370/402 709/253 710/306 710/310 710/311 710/52 710/53 710/100 710/33 710/307 340/2.1 712/29 713/322 713/501 713/600).ccls.	16596

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DB=PGPB, USPT, USOC; PLUR=YES; OP=OR

<u>L7</u> 710/306,310,311,52,53,100,33,307;713/322,501,600;712/29;709/253;375/354;370/230,232,235,401,402;340/2.1 *DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L6 L4 and bridge

DB=PGPB, USPT, USOC; PLUR=YES; OP=OR

L5 L4 and bridge

L4 L1 same multiple

L3 L1 same multiple same (empt\$3 or free)

DB=PGPB; PLUR=YES; OP=OR

<u>L2</u> L1 same multiple same (empt\$3 or free)

<u>L1</u> synchronous\$3 same asynchronous\$3 same (rate or speed)

Search Results -

Terms	Documents
L5 and L7	2

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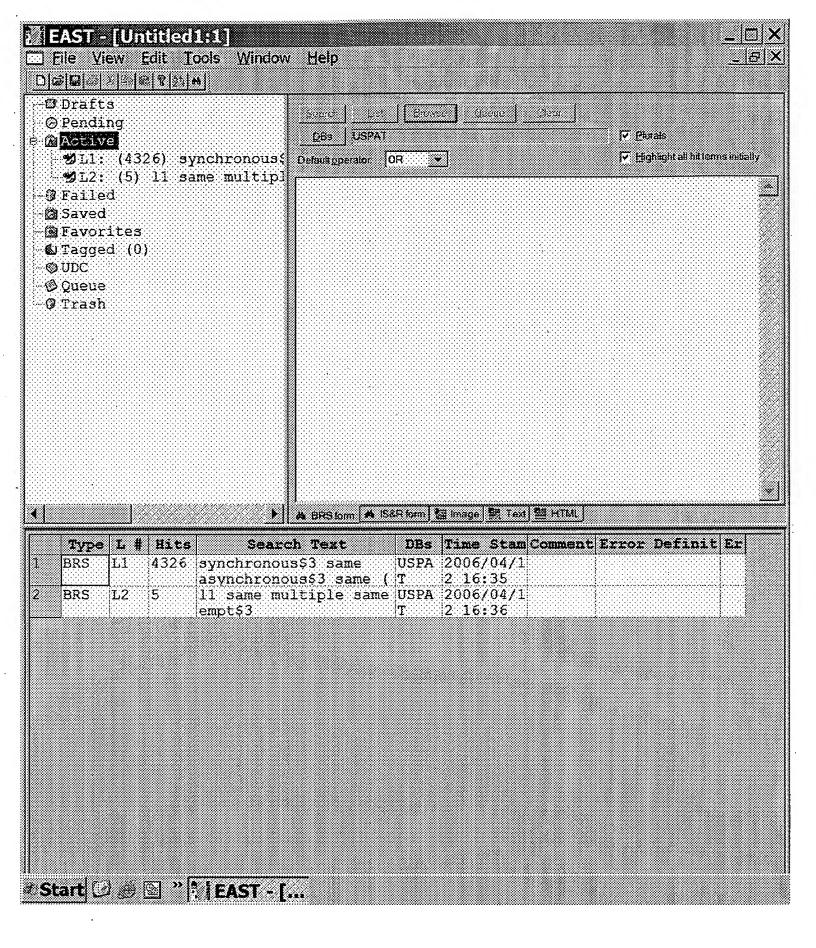
<u>Set</u>

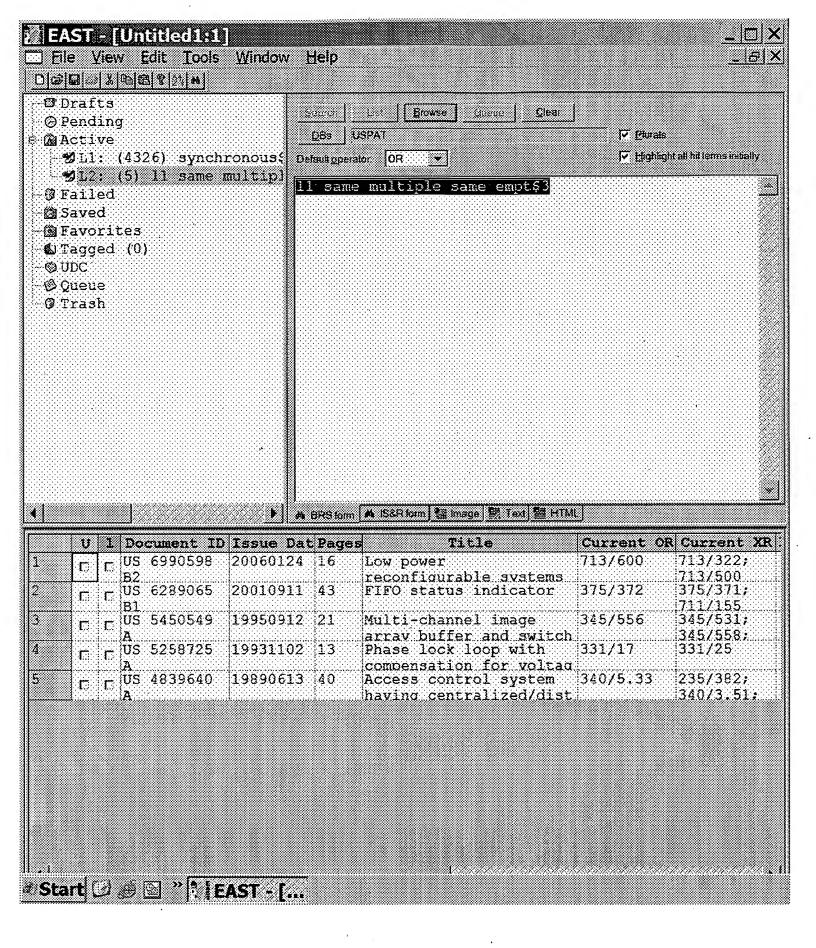
Name Query

side by side

DB=PGPB, USPT, USOC; PLUR=YES; OP=OR

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- <u>L7</u> 710/306,310,311,52,53,100,33,307;713/322,501,600;712/29;709/253;375/354;370/230,232,235,401,402,340/2.1
- DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
- L6 L4 and bridge
- DB=PGPB, USPT, USOC; PLUR=YES; OP=OR
- L5 L4 and bridge
- <u>L4</u> L1 same multiple
- L3 L1 same multiple same (empt\$3 or free)
- DB=PGPB; PLUR=YES; OP=OR
- L2 L1 same multiple same (empt\$3 or free)
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Memory faults in asynchronous microprocessors

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This paper appears in: Advanced Research in Asynchronous Circuits and Systems, 1999, Proceedings, Fifth International

Symposium on

Publication Date: 19-21 April 1999

On page(s): 71 - 80

Number of Pages: xii+251

Meeting Date: 04/19/1999 - 04/21/1999

Location: Barcelona

INSPEC Accession Number:6415609

Digital Object Identifier: 10.1109/ASYNC.1999.761524

Posted online: 2002-08-06 22:28:48.0

Abstract

Although a large number of asynchronous microprocessors have now been designed, relatively few have attempted to handle memory faults. Memory faults create problems for the design of any pipelined system which are exacerbated by the non-deterministic nature of an asynchronous processor. This paper describes these problems as encountered in the design of asynchronous ARM processors and discusses their specific solutions in the AMULET3 processor. Different mechanisms were used, as expedient, to maintain coherency for the various state-holding elements within the processor; these include register renaming and history buffering in addition to resource locking

Index Terms

Inspec

Controlled Indexing

asynchronous circuits buffer storage microprocessor chips pipeline processing

Non-controlled Indexing

AMULET3 processor ARM processors asynchronous microprocessors history buffering memory faults pipelined system register renaming resource locking

Author Keywords

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